# TS64MLR72V6F

**168PIN PC133 Registered DIMM**
**512MB With 32M X8 CL3**

## Description

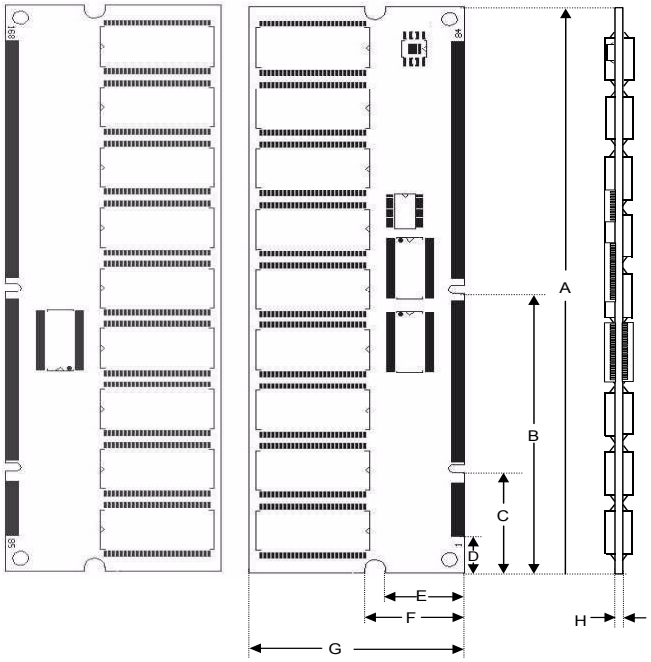
The TS64MLR72V6F is a 64M bit x 72 Synchronous Dynamic RAM high-density memory registered DIMM module. The TS64MLR72V6F consists of 18pcs 16Mx8 bits Synchronous DRAMs, 3pcs drive ICs for input control signal, 1pc PLL and a 2048 bits serial EEPROM on a 168-pin printed circuit board. The TS64MLR72V6F is a Dual In-Line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

## Features

- RoHS compliant products.
- Performance Range: PC-133
- Burst Mode Operation.
- Auto and Self Refresh.
- DQM Byte Masking (Read/Write)
- Serial Presence Detect (SPD) with serial EEPROM
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8 & Full Page)
  Data Sequence (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

## Placement




**PCB: 09-0872**

## Dimensions

| Side | Millimeters | Inches |
|---|---|---|
| A | 133.35±0.40 | 5.250±0.016 |
| B | 65.67 | 2.585 |
| C | 23.49 | 0.925 |
| D | 8.89 | 0.350 |
| E | 15.80 | 0.622 |
| F | 19.80 | 0.780 |
| G | 43.00±0.20 | 1.693±0.008 |
| H | 1.27±0.10 | 0.050±0.004 |

**(Refer Placement)**

## Pin Identification

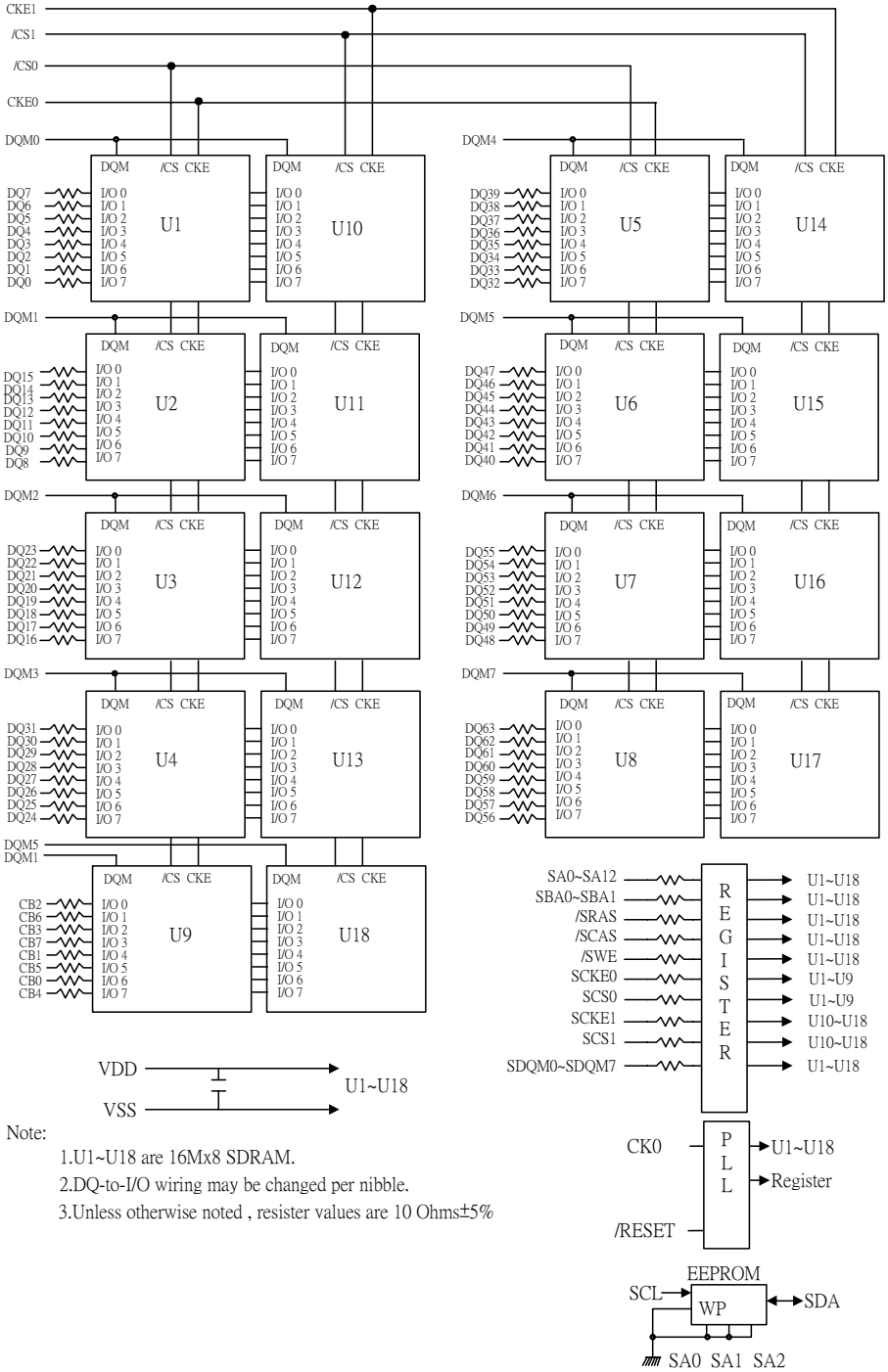
| Symbol | Function |
|---|---|
| SA0~SA12 | Address Input |
| SBA0,SBA1 | Select Bank Address |
| SD0~SD63 | Data Input / Output. |
| SCB0~SCB7 | Check bit (data-in / data-out) |
| SCK0 | Clock Input. |
| SCKE0 | Clock Enable Input. |
| /SCS0~SCS3 | Chip Select Input. |
| /SRAS | Row Address Strobe |
| /SCAS | Column Address Strobe |
| /SWE | Write Enable |
| SDQM0~SDQM7 | Data (DQ) Mask |
| SREGE | Register Enable |
| EA0~EA2 | Address in EEPROM |
| SCL | Serial PD Clock |
| SDA | Serial PD Add/Data input/output |
| Vcc | +3.3 Voltage Power Supply |
| Vss | Ground |
| NC | No Connection |

**Pinouts:**

| Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name |
|---|---|---|---|---|---|---|---|
| 01 | Vss | 43 | Vss | 85 | Vss | 127 | Vss |
| 02 | DQ0 | 44 | NC | 86 | DQ32 | 128 | CKE0 |
| 03 | DQ1 | 45 | /CS2 | 87 | DQ33 | 129 | */CS3 |
| 04 | DQ2 | 46 | DQM2 | 88 | DQ34 | 130 | DQM6 |
| 05 | DQ3 | 47 | DQM3 | 89 | DQ35 | 131 | DQM7 |
| 06 | Vcc | 48 | NC | 90 | Vcc | 132 | *A13 |
| 07 | DQ4 | 49 | Vcc | 91 | DQ36 | 133 | Vcc |
| 08 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 09 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | *CB2 | 94 | DQ39 | 136 | *CB6 |
| 11 | DQ8 | 53 | *CB3 | 95 | DQ40 | 137 | *CB7 |
| 12 | Vss | 54 | Vss | 96 | Vss | 138 | Vss |
| 13 | DQ9 | 55 | DQ16 | 97 | DQ41 | 139 | DQ48 |
| 14 | DQ10 | 56 | DQ17 | 98 | DQ42 | 140 | DQ49 |
| 15 | DQ11 | 57 | DQ18 | 99 | DQ43 | 141 | DQ50 |
| 16 | DQ12 | 58 | DQ19 | 100 | DQ44 | 142 | DQ51 |
| 17 | DQ13 | 59 | Vcc | 101 | DQ45 | 143 | Vcc |
| 18 | Vcc | 60 | DQ20 | 102 | Vcc | 144 | DQ52 |
| 19 | DQ14 | 61 | NC | 103 | DQ46 | 145 | NC |
| 20 | DQ15 | 62 | *Vref | 104 | DQ47 | 146 | *Vref |
| 21 | *CB0 | 63 | *CKE1 | 105 | *CB4 | 147 | *REGE |
| 22 | *CB1 | 64 | Vss | 106 | *CB5 | 148 | Vss |
| 23 | Vss | 65 | DQ21 | 107 | Vss | 149 | DQ53 |
| 24 | NC | 66 | DQ22 | 108 | NC | 150 | DQ54 |
| 25 | NC | 67 | DQ23 | 109 | NC | 151 | DQ55 |
| 26 | Vcc | 68 | Vss | 110 | Vcc | 152 | Vss |
| 27 | /WE | 69 | DQ24 | 111 | /CAS | 153 | DQ56 |
| 28 | DQM0 | 70 | DQ25 | 112 | DQM4 | 154 | DQ57 |
| 29 | DQM1 | 71 | DQ26 | 113 | DQM5 | 155 | DQ58 |
| 30 | /CS0 | 72 | DQ27 | 114 | */CS1 | 156 | DQ59 |
| 31 | NC | 73 | Vcc | 115 | /RAS | 157 | Vcc |
| 32 | Vss | 74 | DQ28 | 116 | Vss | 158 | DQ60 |
| 33 | A0 | 75 | DQ29 | 117 | A1 | 159 | DQ61 |
| 34 | A2 | 76 | DQ30 | 118 | A3 | 160 | DQ62 |
| 35 | A4 | 77 | DQ31 | 119 | A5 | 161 | DQ63 |
| 36 | A6 | 78 | Vss | 120 | A7 | 162 | Vss |
| 37 | A8 | 79 | *CLK2 | 121 | A9 | 163 | *CLK3 |
| 38 | A10/AP | 80 | NC | 122 | BA0 | 164 | NC |
| 39 | BA1 | 81 | NC | 123 | A11 | 165 | SA0 |
| 40 | Vcc | 82 | SDA | 124 | Vcc | 166 | SA1 |
| 41 | Vcc | 83 | SCL | 125 | *CLK1 | 167 | SA2 |
| 42 | CLK0 | 84 | Vcc | 126 | *A12 | 168 | Vcc |

*** Please refer Block Diagram**

## Block Diagram




Note:

1.U1~U18 are 16Mx8 SDRAM.

2.DQ-to-I/O wiring may be changed per nibble.

3.Unless otherwise noted , resister values are 10 Ohms±5%


This technical information is based on industry standard data and tests believed to be reliable. However , Transcend makes no warranties, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | VIN, VOUT | -1.0~4.6 | V |
| Voltage on VDD supply to Vss | VDD, VDDQ | -1.0~4.6 | V |
| Storage temperature | TSTG | -55~+150 | °C |
| Power dissipation | PD | 18 | W |
| Short circuit current | IOS | 50 | mA |
| Operating Temperature | $T_A$ | 0~70 | °C |

**Note:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

**Recommended operating conditions (Voltage referenced to Vss = 0V, $T_A$ = 0 to 70°C)**

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V | |
| Input high voltage | $V_{IH}$ | 2.0 | 3.0 | $V_{DD}$+0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | -0.3 | 0 | 0.8 | V | 2 |
| Output high voltage | $V_{OH}$ | 2.4 | - | - | V | IOH=-2mA |
| Output low voltage | $V_{OL}$ | - | - | 0.4 | V | IOL=2mA |
| Input leakage current | $I_{IL}$ | -10 | - | 10 | uA | 3 |

**Note:** 1. $V_{IH}$ (max) = 5.6V AC .The overshoot voltage duration is ≤ 3ns.
2. $V_{IL}$ (min) = -2.0V AC .The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ $V_{IN}$ ≤ $V_{DDQ}$.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE ($V_{DD}$ = 3.3V, TA = 23°C, f = 1MHz, $V_{REF}$ = 1.4V±200mV)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance ($SA_0$~$SA_{12}$, $SBA_0$~ $SBA_1$) | $C_{IN1}$ | 85 | 105 | pF |
| Input capacitance (/SRAS, /SCAS, /SWE) | $C_{IN2}$ | 85 | 105 | pF |
| Input capacitance (SCKE0) | $C_{IN3}$ | 50 | 65 | pF |
| Input capacitance (SCLK0) | $C_{IN4}$ | 40 | 45 | pF |
| Input capacitance (/SCS0~/SCS3) | $C_{IN5}$ | 30 | 40 | pF |
| Input capacitance (SDQM0~SDQM7) | $C_{IN6}$ | 25 | 30 | pF |
| Data input/output capacitance (SD0~SD63) | $C_{OUT}$ | 10 | 15 | pF |
| Data input/output capacitance (SCB0~SCB7) | $C_{OUT}1$ | 10 | 15 | pF |

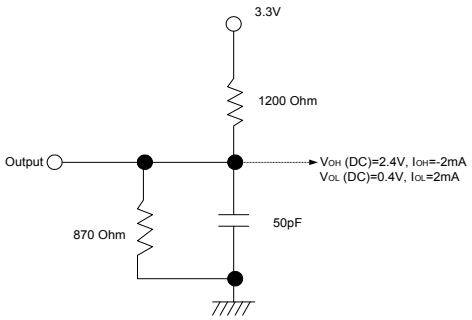
## DC CHARACTERISTICS (Recommended operating condition unless otherwise noted, $T_A$ = 0 to 70°C)

| Parameter | Symbol | Test Condition | CAS Latency | Value | Unit | Note |
|---|---|---|---|---|---|---|
| Operating Current (One Bank Active) | $I_{CC1}$ | Burst Length =1<br>$t_{RC} \geq t_{RC}$(min)<br>$I_{OL}$=0mA | | 1,350 | | |
| Precharge Standby Current in power-down mode | $I_{CC2}$**P** | CKE≤$V_{IL}$(max), $t_{CC}$=10ns | | 36 | mA | 3 |
| | $I_{CC2}$**PS** | CKE & CLK≤$V_{IL}$(max), $t_{CC}$=∞ | | 36 | | |
| Precharge Standby Current in non power-down mode | $I_{CC2}$**N** | CKE≥$V_{IH}$(min), /CS≥$V_{IH}$(min), $t_{CC}$=10ns<br>Input signals are changed one time during 30ns | | 288 | mA | 3 |
| | $I_{CC2}$**NS** | CKE≥$V_{IH}$(min), CLK≤$V_{IL}$(max), $t_{CC}$=∞<br>Input signals are stable | | 252 | | |
| Active Standby Current in power-down mode | $I_{CC3}$**P** | CKE≤$V_{IL}$(max), $t_{CC}$=10ns | | 108 | mA | 3 |
| | $I_{CC3}$**PS** | CKE & CLK≤$V_{IL}$(max), $t_{CC}$=∞ | | 108 | | |
| Active Standby Current in non power-down mode (One Bank Active) | $I_{CC3}$**N** | CKE≥$V_{IH}$(min), /CS≥$V_{IH}$(min), $t_{CC}$=10ns<br>Input signals are changed one time during 20ns | | 540 | mA | 3 |
| | $I_{CC3}$**NS** | CKE≥$V_{IH}$(min), CLK≤$V_{IL}$(max), $t_{CC}$=∞<br>Input signals are stable | | 450 | | |
| Operating Current (Bust Mode) | $I_{CC4}$ | $I_{OL}$= 0 mA<br>Page Burst<br>$t_{CCD}$ = 2CLKs | | 1,530 | mA | 1 |
| Refresh Current | $I_{CC5}$ | $t_{RC} \geq t_{RC}$(min) | | 2,160 | mA | 2,3 |
| Self Refresh Current | $I_{CC6}$ | CKE≤0.2V | | 90 | mA | 3 |

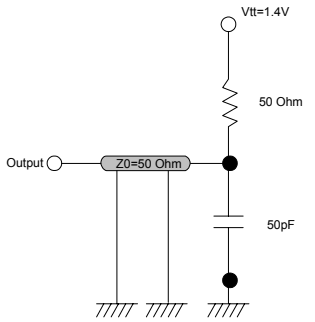
**Note:** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## AC OPERATING TEST CONDITIONS ($V_{DD}$ = 3.3V±0.3V, TA = 0 to 70°C)

| Parameter | Value | Unit |
|---|---|---|
| AC Input levels ($V_{IH}/V_{IL}$) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | tr/tf=1/1 | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig. 2 | |



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

## OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Row active to row active delay | $t_{RRD}$(min) | 15 | ns | 1 |
| /RAS to /CAS delay | $t_{RCD}$(min) | 20 | ns | 1 |
| Row precharge time | $t_{RP}$(min) | 20 | ns | 1 |
| Row active time | $t_{RAS}$(min) | 45 | ns | 1 |
| | $t_{RAS}$(max) | 100 | us | |
| Row cycle time | $t_{RC}$(min) | 65 | ns | 1 |
| Last data in to new col. address delay | $t_{CDL}$(min) | 1 | CLK | 2 |
| Last data in to row precharge | $t_{RDL}$(min) | 2 | CLK | 2 |
| Last data in to burst stop | $t_{BDL}$(min) | 1 | CLK | 2 |
| Col. address to col. address delay | $t_{CCD}$(min) | 1 | CLK | 3 |
| Number of valid output data | CAS latency=3 | 2 | ea | 4 |

**Note:** 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

**AC CHARACTERISTICS (AC operating conditions unless otherwise noted)**

**Refer to the individual component, not the whole module.**

| Parameter | | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| CLK cycle time | CAS latency=3 | tCC | 7.5 | 1000 | ns | 1 |
| CLK to valid output delay | CAS latency=3 | tSAC | | 5.4 | ns | 1, 2 |
| Output data hold time | CAS latency=3 | tOH | 2.7 | | ns | 1, 2 |
| CLK high pulse width | | tCH | 2.5 | | ns | 3 |
| CLK low pulse width | | tCL | 2.5 | | ns | 3 |
| Input setup time | | tSS | 1.5 | | ns | 3 |
| Input hold time | | tSH | 0.8 | | ns | 3 |
| CLK to output in Low-Z | | tSLZ | 1 | | ns | 2 |
| CLK to outputin Hi-Z | CAS latency=3 | tSHZ | | 5.4 | ns | 1 |

**Note:** 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf)= 1ns.

If tr & tf is longer than 1ns, transient time compensation should be considered,

i.e., [(tr + tf)/2-1]ns should be added to the parameter.

## SIMPLIFIED TRUTH TABLE

| COMMAND | | | SCKEn-1 | SCKEn | /SCS | /SRAS | /SCAS | /SWE | SDQM | $SBA_{0,1}$ | $SA_{10}$/AP | $SA_{12}$,$A_{11}$,$SA_0$~$SA_9$ | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Mode Register Set | | H | X | L | L | L | L | X | OP CODE | | | 1,2 |
| Refresh | Auto Refresh | | H | H | L | L | L | H | X | X | | | 3 |
| | Self Refresh | Entry | | L | | | | | | | | | 3 |
| | | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank Active & Row Adders. | | | H | X | L | L | H | H | X | V | Row Address | | |
| Read & Column Address | Auto Precharge Disable | | H | X | L | H | L | H | X | V | L | Column Address ($SA_0$~$SA_9$,$SA_{11}$) | 4 |
| | Auto Precharge Enable | | | | | | | | | | H | | 4, 5 |
| Write & Column Address | Auto Precharge Disable | | H | X | L | H | L | L | X | V | L | Column Address ($SA_0$~$SA_9$,$SA_{11}$) | 4 |
| | Auto Precharge Enable | | | | | | | | | | H | | 4, 5 |
| Burst Stop | | | H | X | L | H | H | L | X | X | | | 6 |
| Precharge | Bank Selection | | H | X | L | L | H | L | X | V | L | X | |
| | Both Banks | | | | | | | | | X | H | | |
| Clock Suspend or Active Power Down | Entry | | H | L | H | X | X | X | X | X | | | |
| | | | | | L | V | V | V | | | | | |
| | Exit | | L | H | X | X | X | X | X | | | | |
| Precharge Power Down Mode | Entry | | H | L | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |
| | Exit | | L | H | H | X | X | X | X | | | | |
| | | | | | L | V | V | V | | | | | |
| SDQM | | | H | | | X | | | V | X | | | 7 |
| No Operation Command | | | H | X | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

**Note:**
1. OP Code : Operand Code
   $SA_0$~$SA_{11}$, $SBA_0$~$SBA_1$ : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatically precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at both banks precharge state.
4. $SBA_0$~$SBA_1$: Bank select address.
   If both $SBA_0$ and $SBA_1$ are "Low" at read, write, row active and precharge, bank A is selected.
   If both $SBA_0$ is "Low" and $SBA_1$ is "High" at read, write, row active and precharge, bank B is selected.
   If both $SBA_0$ is "High" and $SBA_1$ is "Low" at read, write, row active and precharge, bank C is selected.
   If both $SBA_0$ and $SBA_1$ are "High" at read, write, row active and precharge, bank D is selected.
   If $SA_{10}$/AP is "High" at row precharge, $SBA_0$ and $SBA_1$ is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. SDQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write SDQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read SDQM latency is 2)

## Serial Presence Detect Specification

| Serial Presence Detect | | | |
|---|---|---|---|
| Byte No. | Function Described | Standard Specification | Vendor Part |
| 0 | Number of Bytes Written into Serial Memory | 128bytes | 80 |
| 1 | Total Number of Bytes of S.P.D Memory | 256bytes | 08 |
| 2 | Fundamental Memory Type | SDRAM | 04 |
| 3 | Number of Row Addresses on this Assembly | 13 | 0D |
| 4 | Number of Column Addresses on this Assembly | 10 | 0A |
| 5 | Number of Module Banks on this Assembly | 2 bank | 02 |
| 6 | Data Width of this Assembly | 72bits | 48 |
| 7 | Data Width Continuation | 0 | 00 |
| 8 | Voltage Interface Standard of this Assembly | LVTTL3.3V | 01 |
| 9 | SDRAM Cycle Time (highest CAS latency) | 7.5ns | 75 |
| 10 | SDRAM Access from Clock (highest CL) | 5.4ns | 54 |
| 11 | DIMM configuration type (non-parity, ECC) | ECC | 02 |
| 12 | Refresh Rate Type | 7.8us/Self Refresh | 82 |
| 13 | Primary SDRAM Width | X8 | 08 |
| 14 | Error Checking SDRAM Width | X8 | 08 |
| 15 | Min Clock Delay Back to Back Random Address | 1 clock | 01 |
| 16 | Burst Lengths Supported | 1,2,4,8 & Full page | 8F |
| 17 | Number of banks on each SDRAM device | 4 bank | 04 |
| 18 | CAS # Latency | 3 | 04 |
| 19 | CS # Latency | 0 clock | 01 |
| 20 | Write Latency | 0 clock | 01 |
| 21 | SDRAM Module Attributes | Registered DQM, address/control inputs and on-card PLL | 16<br>16 |
| 22 | SDRAM Device Attributes: General | Prec All, Auto Prec, R/W Burst | 0E |
| 23 | SDRAM Cycle Time (2nd highest CL) | 0ns | 00 |
| 24 | SDRAM Access from Clock (2nd highest CL) | 0ns | 00 |
| 25 | SDRAM Cycle Time (3rd highest CL) | 0ns | 00 |
| 26 | SDRAM Access from Clock (3rd highest CL) | 0ns | 00 |
| 27 | Minimum Row Precharge Time | 20ns | 14 |
| 28 | Minimum Row Active to Row Activate | 15ns | 0F |
| 29 | Minimum RAS to CAS Delay | 20ns | 14 |
| 30 | Minimum RAS Pulse Width | 45ns | 2D |
| 31 | Density of Each Bank on Module | 256MB | 40 |
| 32 | Command/Address Setup Time | 1.5ns | 15 |
| 33 | Command/Address Hold Time | 0.8ns | 08 |
| 34 | Data Signal Setup Time | 1.5ns | 15 |
| 35 | Data Signal Hold Time | 0.8ns | 08 |

| | | | |
|---|---|---|---|
| 36-61 | Superset Information | - | 00 |
| 62 | SPD Data Revision Code | JEDEC 2 | 02 |
| 63 | Checksum for Bytes 0-62 | - | E9 |
| 64-71 | Manufacturers JEDEC ID Code per JEP-108E | Transcend | 7F, 4F |
| 72 | Manufacturing Location | T | 54 |
| 73-90 | Manufacturers Part Number | TS64MLR72V6F | 54 53 36 34 4D 4C<br>52 37 32 56 36 46<br>20 20 20 20 20 20 |
| 91-92 | Revision Code | - | 0 |
| 93-94 | Manufacturing Date | By Manufacturer | Variable |
| 95-98 | Assembly Serial Number | By Manufacturer | Variable |
| 99-125 | Manufacturer Specific Data | - | 0 |
| 126 | Intel Specification Frequency | - | 64 |
| 127 | Intel Specification CAS# Latency/Clock Signal Support | CL=3 Clock 0 | 84 |
| 128~ | Unused Storage Locations | Open | FF |